Features

- **Digital Self-supervising Watchdog with Hysteresis**
- **One 150-mA Output Driver for Relay**
- **One High-side Driver for N-channel Power FET**
- **Positive and Negative Enable Output**
- **Positive and Negative Reset Output**
- **Over/Under-voltage Detection**
- **Relay and Power FET Outputs Protected Against Standard Transients and 55-V Load Dump**

Fail-safe IC with High-side and Relay Driver

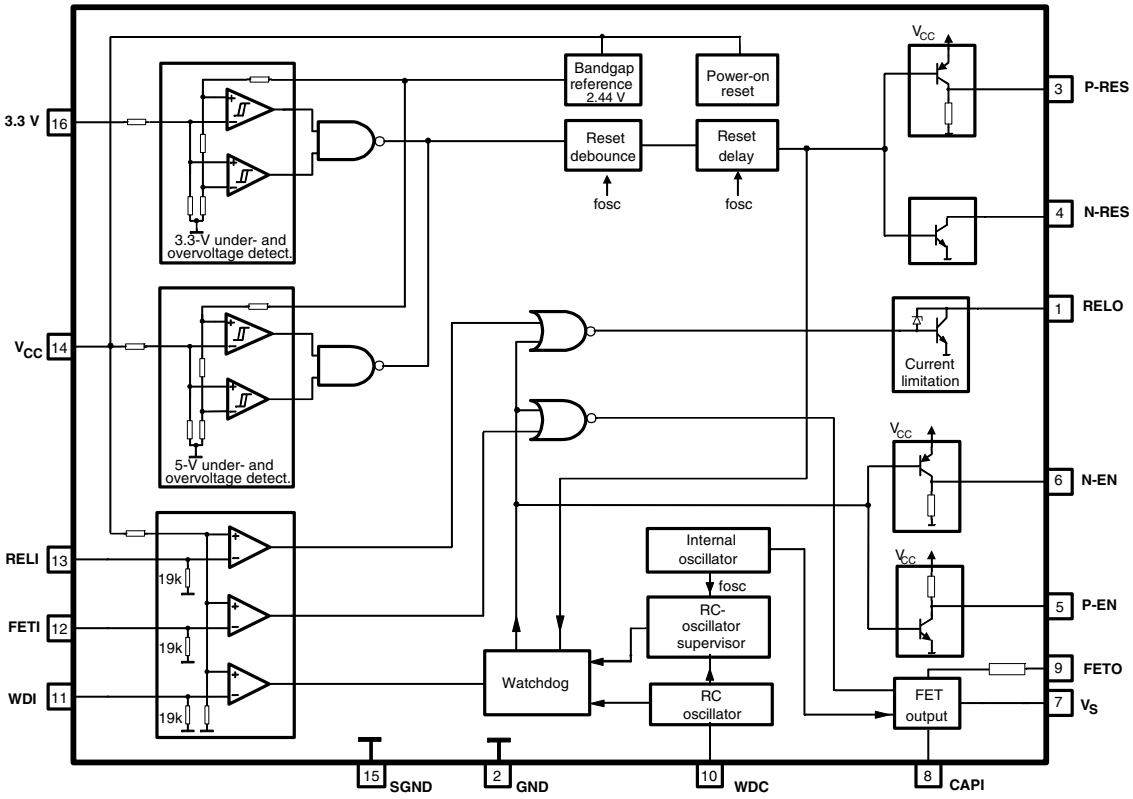
U6813B

1. Description

The function of microcontrollers in safety-critical applications (e.g., anti-lock systems) needs to be monitored permanently. Usually, this task is accomplished by an independent watchdog timer. The monolithic IC U6813B, designed in bipolar technology and qualified according to the needs of the automotive industry, includes such a watchdog timer and provides additional features for added value. With the help of integrated driver stages, it is easy to control safety-related functions of a relay and of an N-channel power MOSFET in high-side applications. In case of a microcontroller malfunction or supply-voltage anomalies, the U6813B provides positive and negative reset and enable output signals. This flexibility guarantees a broad range of applications. The U6813B is based on of Atmel's fail-safe ICs U6808B and U6809B.

Rev. 4543B–AUTO–10/05

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO16

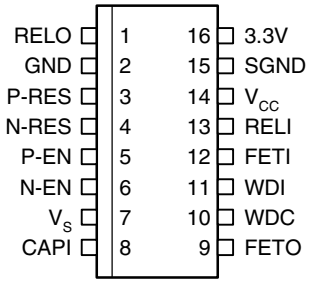


Table 2-1. Pin Description

Pin	Symbol	Description	Function	Type
1	RELO	Open-collector output driver	Fail-safe relay driver	Driver on: L
2	GND	Supply	General ground	
3	P-RES	Digital output	Positive reset signal	Reset: H
4	N-RES	Digital output	Negative reset signal	Reset: L
5	P-EN	Digital output	Positive enable signal	Enable: H
6	N-EN	Digital output	Negative enable signal	Enable: L
7	V_S	Battery supply	Voltage for charge pump	
8	CAPI	Analog input	Input bootstrap capacitor	
9	FETO	Power FET output	High voltage for N-channel FET	
10	WDC	Analog input	External RC for watchdog timer	
11	WDI	Digital input	Watchdog trigger signal	Pulse sequence
12	FETI	Digital input	Activation of power FET	FET on: H
13	RELI	Digital input	Activation of relay driver	Driver on: H
14	V_{CC}	Supply	5-V supply	
15	SGND	Supply	Sense ground, reference for V_{CC} and 3.3 V	
16	3.3V	Analog input	3.3-V supply	

3. Fail-safe Functions

A fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g., short circuit), ensuring that a microcontroller system does not reach a “critical status”. A critical status means, for example, if the system is not able to switch off the relay or disable the power MOSFET, or if the system is not able to provide a signal to the microcontroller via ENABLE- and RESET-outputs in the case of a fault condition. The U6813B is designed to handle those fault conditions according to Table 3-1 for a maximum of system safety.

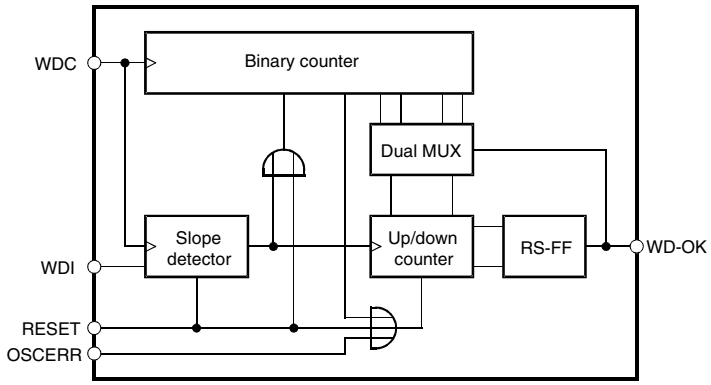
Table 3-1. Truth Table

VCC	3.3V	WDI	RELI	FETI	RELO	FETO	N-RES	P-RES	P-EN(2)	N-EN(3)
ok	ok	ok	H	x	on	x	H	L	H	L
ok	ok	ok	L(1)	x	off	x	H	L	H	L
ok	ok	ok	x	H	x	on	H	L	H	L
ok	ok	ok	x	L (1)	x	off	H	L	H	L
ok	ok	wrong	x	x	off	off	H	L	L	H
x	wrong	x	x	x	off	off	L	H	L	H
wrong	x	x	x	x	off	off	L	H	L	H

Notes: 1. default state at open input
2. P-EN disable: low
3. N-EN disable: high

4. Watchdog Description

Figure 4-1. Watchdog Block Diagram



The microcontroller is monitored by a digital window watchdog which accepts an incoming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the watchdog’s time window is determined by external R/C components. The following description refers to the watchdog timing diagram with tolerances (see Figure 4-2 on page 5).

4.1 WDI Input (Pin 11)

The microcontroller has to provide a trigger signal with the frequency f_{WDI} which is fed to the WDI input. A positive edge of f_{WDI} detected by a slope detector resets the binary counter and clocks the up/down counter.The latter one counts only from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches status 3, the RS flip-flop is set; see Figure 4-3 (Watchdog state diagram). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency f_{RC} (see WD_OK output) and resets the up/down counter directly.

4.2 WDC Input (Pin 10)

It is to be equiped by external R/C components. By means of an external R/C circuitry, the IC generates a time base (frequency f_{WDC}) independent from the microcontroller. The watchdog's time window refers to a frequency of $f_{WDC} = 100 \times f_{WDI}$.

4.3 OSCERR Input

A smart watchdog has to ensure that internal problems with its own time base are detected and do not lead to an undesired status of the complete system. If the RC oscillator stops oscillating, a signal is fed to the OSCERR input after a time-out delay. It resets the up/down counter and disables the WD-OK output. Without this reset function, the watchdog would freeze its current status when f_{RC} stops.

4.4 RESET Input

During power-on and under/overvoltage detection, a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

4.5 WD-OK Output

After the up/down counter has reached to status 3 (see Figure 4-3, Watchdog State Diagram), the RS flip-flop is set and the WD-OK output becomes logic "1". As WD-OK is directly connected to the enable pins, the open-collector output P-EN provides also logic "1" while a logic "0" is available at N-EN output. If on the other hand the up/down counter is decremented to "0", the RS flip-flop is reset, the WD-OK output and the P-EN output are logic "0" and N-EN output is logic "1". The WD-OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger, thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal "good or false". The WD-OK signal is also reset in case the watchdog counter is not reset after 250 clocks (missing trigger signal).

Figure 4-2. Watchdog Timing Diagram with Tolerances

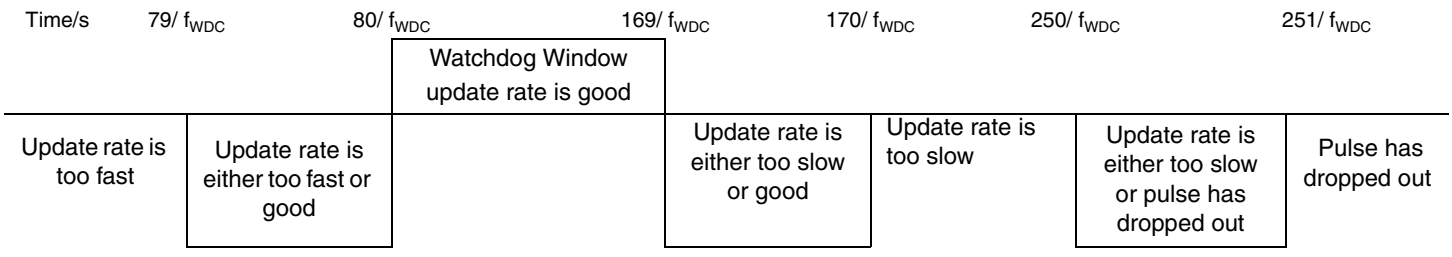
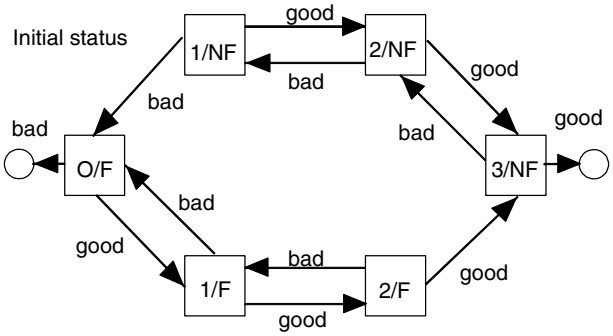


Figure 4-3. Watchdog State Diagram



4.6 Explanation

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an “F” and a no-fault status is indicated by an “NF”. When the watchdog is powered up initially, the counter starts at the 0/F block (initial state). “Good” indicates that a pulse has been received whose width resides within the timing window. “Bad” indicates that a pulse has been received whose width is either too short or too long.

4.7 Watchdog Window Calculation

Example with recommended values
C_{osc} = 6.8 nF (should be preferably 10%, NPO)
R_{osc} = 36 kΩ (can be 5%, R_{osc} < 200 kΩ due to leakage current and humidity)

RC oscillator
t_{WDC} (s) = 10^{-3} [C_{osc} (nF) [(0.00078 R_{osc} (kΩ)) + 0.0005]]
f_{WDC} (Hz) = 1/(t_{WDC})

Watchdog WDI
f_{WDI} (Hz) = 0.01 f_{WDC}
t_{WDC} = 200 µs → f_{WDC} = 5 kHz
f_{WDI} = 50 Hz → t_{WDI} = 20 ms

WDI pulse width for fault detection after 3 pulses:

Upper watchdog window

Minimum: 169/ f_{WDC} = 33.8 ms→ f_{WDC}/169 = 29.55 Hz
Maximum: 170/ f_{WDC} = 34 ms → f_{WDC}/170 = 29.4 Hz

Lower watchdog window

Minimum: 79/ f_{WDC} = 15.8 ms → f_{WDC}/79 = 63.3 Hz
Maximum: 80/ f_{WDC} = 16 ms → f_{WDC}/80 = 62.5 Hz

WDI dropouts for immediate fault detection:

Minimum: 250/ f_{WDC} = 50.0 ms
Maximum: 251/ f_{WDC} = 50.2 ms

Remarks to reset relay

The duration of the over- or undervoltage pulses determines the enable- and reset outputs. A pulse duration shorter than the debounce time has no effect on the outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a second delay time is triggered. Therefore, the total reset delay time can be longer than specified in the data sheet.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage range	V_S	–0.2 to +26	V
Power dissipation V_S = 5V; T_{amb} = –40°C V_S = 5V; T_{amb} = 125°C	 P_{tot} P_{tot}	 250 150	 mW mW
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to +125	°C
Storage temperature range	T_{stg}	–55 to +155	°C

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	110	K/W

7. Electrical Characteristics

V_{CC} = 5V, T_{amb} = –40 to +125°C; reference pin is GND or SGND (over- and under-voltage detection);
f_{intern} = 200 kHz +50%/–45%, f_{WDC} = 5 kHz ±10%; f_{WDI} = 50 Hz, bootstrap capacitor C_{Boot} = 47 nF at pin CAPI

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Supply**								
1.1	Operation-voltage range		14	V_{CC}	4.5		5.5	V	D
1.2	Operation-voltage range of RESET outputs		14	V_{CC}	1.1		18.0	V	A
1.3	Current consumption	V = 5.25V, Relay on T_{amb} = –40° C T_{amb} = +125° C	14	I_{CC} I_{CC}			15 10	mA mA	A
2	**Digital Input WDI**								
2.1	Detection low		11	V_{WDI}	–0.2		$0.3 \times V_{CC}$	V	D
2.2	Detection high		11	V_{WDI}	$0.7 \times V_{CC}$		V_{CC} + 0.2V	V	D
2.3	Internal pull-down resistor		11	R_{INT11}	10		40	kΩ	A
2.4	Input current low	Input voltage = 0V	11	I_{WDI}	–5		5	µA	A
2.5	Input current high	Input voltage = 5V	11	I_{WDI}	100		550	µA	A
3	**Digital Input RELI**								
3.1	Detection low		13	V_{RELI}	–0.2		$0.3 \times V_{CC}$	V	D
3.2	Detection high		13	V_{RELI}	$0.7 \times V_{CC}$		V_{CC} + 0.2V	V	D
3.3	Internal pull-down resistor		13	R_{INT13}	10		40	kΩ	A
3.4	Input current low	Input voltage = 0V	13	I_{RELI}	–5		5	µA	A
3.5	Input current high	Input voltage = 5V	13	I_{RELI}	100		550	µA	A
4	**Digital Input FETI**								
4.1	Detection low		12	V_{FETI}	–0.2		$0.3 \times V_{CC}$	V	A
4.2	Detection high		12	V_{FETI}	$0.7 \times V_{CC}$		V_{CC} + 0.2V	V	A
4.3	Internal pull-down resistor		12	R_{INT12}	10		40	kΩ	A
4.4	Input current low	Input voltage = 0V	12	I_{FETI}	–5		5	µA	A
4.5	Input current high	Input voltage = 5V	12	I_{FETI}	100		550	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If V_S > 26 V the current has to be limited at 5 mA by an external resistor.

7. Electrical Characteristics (Continued)

V_{CC} = 5V, T_{amb} = –40 to +125°C; reference pin is GND or SGND (over- and under-voltage detection);
f_{intern} = 200 kHz +50%/–45%, f_{WDC} = 5 kHz ±10%; f_{WDI} = 50 Hz, bootstrap capacitor C_{Boot} = 47 nF at pin CAPI

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**Digital Output N-RES (Open Collector)**								
5.1	Saturation voltage low	$I_{reset} \leq 2.5$ mA	4	V_{SAT4}			0.5	V	A
5.2	Leakage current	at 5V, high state	4	I_{LEAK4}			0.5	µA	A
5.3	Reset debounce time (switch to low)	Over- or undervoltage	4	t_{DEB4}	120	320	500	µs	A
5.4	Reset delay (switch back to high)	Over- or undervoltage	4	t_{DEL4}		50		ms	A
6	**Digital Output P-RES (Internal Pull-down Resistor)**								
6.1	Saturation voltage high	$I_{reset} \leq 0.3$ mA	3	V_{SAT3}	V_{CC}– 0.5V		V_{CC}	V	A
6.2	Leakage current	at 0V, low state	3	I_{LEAK3}			0.5	µA	A
6.3	Internal pull-down resistor	at 5V	3	R_{INT3}	25		100	kΩ	A
6.4	Reset debounce time (switch to low)	Over- or undervoltage	3	t_{DEB3}	120	320	500	µs	A
6.5	Reset delay (switch back to high)	Over- or undervoltage	3	t_{DEL3}		50		ms	A
7	**Digital Output N-EN (with Open Collector and Internal Pull-down Resistor)**								
7.1	Saturation voltage high	I ≤ 1 mA	6	V_{SAT6}	V_{CC} – 0.5V		V_{CC}	V	A
7.2	Leakage current	at 0V, low state	6	I_{LEAK6}			0.5	µA	A
7.3	Internal pull-down resistor	at 5V	6	R_{INT6}	25		100	kΩ	A
7.4	Enable debounce time (switch to low)	Over- or undervoltage	6	t_{DEB6}	120	320	500	µs	A
7.5	Enable delay (switch back to high)	Over- or undervoltage	6	t_{DEL6}		85		ms	A
8	**Digital Output P-EN (Internal Pull-up Resistor)**								
8.1	Saturation voltage high	I ≤ 3 mA	5	V_{SAT5}			0.5	V	A
8.2	Leakage current	at 5V, high state	5	I_{LEAK5}			0.5	µA	A
8.3	Internal pull-up resistor	at 0V	5	R_{INT5}	12.5		50	kΩ	A
8.4	Enable debounce time (switch to high)	Over- or undervoltage	5	t_{DEB5}	120	320	500	µs	A
8.5	Enable delay (switch back to low)	Over- or undervoltage	5	t_{DEL5}		85		ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If V_S > 26 V the current has to be limited at 5 mA by an external resistor.

7. Electrical Characteristics (Continued)

V_{CC} = 5V, T_{amb} = –40 to +125°C; reference pin is GND or SGND (over- and under-voltage detection);
f_{intern} = 200 kHz +50%/–45%, f_{WDC} = 5 kHz ±10%; f_{WDI} = 50 Hz, bootstrap capacitor C_{Boot} = 47 nF at pin CAPI

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	**Relay Driver (RELO)**								
9.1	Saturation voltage	I ≤ 150 mA	1	V_{SAT1}	0.1		0.5	V	A
9.2	Current limitation		1	I_{LIM}	150		300	mA	A
9.3	Internal clamping voltage		1	V_{CL}	26		30	V	A
9.4	Turn-off energy		1		30			mJ	C
9.5	Leakage current	V_{Batt} = 16V V_{Batt} = 26V at 25°C	1	I_{LEAK1} I_{LEAK1}			20 200	µA µA	A
10	**Power-FET Output FETO (Maximum Load Capacitor at FET Gate 470 pF, Charge-pump Frequency 110 to 300 kHz)**								
10.1	Output voltage	V_S = 9V to 15V	9	V_{OUT9}	V_S + 10V		V_S + 15V	V	A
10.2	Operation range		7	V_S	9		20	V	A
10.3	Overvoltage shut-down		7	V_S	20		24	V	A
10.4	Internal clamping voltage		9	V_{CL}	26		30	V	A
10.5	On/off frequency		9	f			200	Hz	A
10.6	Maximum current	FETO	9	I_{FETO}	10			µA	A
11	**Battery Supply**								
11.1	Internal clamping voltage		7	V_{CL}	26		30	V	A
11.2	Clamping current capability(1)		7	I_{VS}	5			mA	A
11.3	Leakage current	at FETI = low	7	I_{LEAVS}			100	µA	A
12	**Reset and V_{CC} Control**								
12.1	Lower reset level	Reference SGND	14	V_{CC}	4.5		4.75	V	A
12.2	Upper reset level	Reference SGND	14	V_{CC}	5.25		5.5	V	A
12.3	Hysteresis		14	V_{HYST14}	25		100	mV	A
12.4	Reset debounce time		14	t_{DEB}	120	320	500	µs	A
12.5	Reset delay		14	t_{DEL}	20	50	80	ms	A
13	**Reset and 3.3V Control**								
13.1	Lower reset level	Reference SGND	16	$V_{3.3V}$	2.97		3.13	V	A
13.2	Upper reset level	Reference SGND	16	$V_{3.3V}$	3.47		3.63	V	A
13.3	Hysteresis		16	V_{HYST16}	15		70	mV	A
13.4	Reset debounce time		16	t_{DEB16}	120	320	500	µs	A
13.5	Reset delay		16	t_{DEL16}	20	50	80	ms	A
13.6	Current		16	$I_{3.3V}$			0.5	mA	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If V_S > 26 V the current has to be limited at 5 mA by an external resistor.

7. Electrical Characteristics (Continued)

V_{CC} = 5V, T_{amb} = –40 to +125°C; reference pin is GND or SGND (over- and under-voltage detection);
f_{intern} = 200 kHz +50%/–45%, f_{WDC} = 5 kHz ±10%; f_{WDI} = 50 Hz, bootstrap capacitor C_{Boot} = 47 nF at pin CAPI

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
14	**RC Oscillator WDC**								
14.1	Oscillator frequency	R_{OSC} = 36 kΩ C_{OSC} = 6.8 nF	10	f_{WDC}	4.5	5	5.5	kHz	A
15	**Watchdog Timing**								
15.1	Power-on-reset prolongation time			t_{POR}	34.3		103.1	ms	A
15.2	Detection time for RC-oscillator fault	V_{CR} = constant		$t_{RCerror}$	81.9		246	ms	A
15.3	Time interval for over/under-voltage detection			$t_{D,OUV}$	0.16		0.64	ms	A
15.4	Reaction time of reset output at over/under voltage			$t_{R,OUV}$	0.187		0.72	ms	A
15.5	Nominal frequency for WDI	f_{RC} = 100 f_{WDI}		f_{WDI}	10		65	Hz	D
15.6	Nominal frequency for WDC	f_{WDI} = 1/100 f_{WDC}		f_{WDC}	1		6.5	kHz	D
15.7	Minimum pulse duration for a guaranteed WDI input-pulse detection	f_{WDC} = 5 kHz		$t_{P,WDI}$	364			µs	A
15.8	Frequency range for a correct WDI signal	f_{WDC} = 5 kHz		f_{WDI}	32.35		56.25	Hz	D
15.9	Number of incorrect WDI trigger counts for locking the outputs			n_{lock}		3			A
15.10	Number of correct WDI trigger counts for releasing the outputs			$n_{release}$		3			A
15.11	Detection time for a stucked WDI signal	V_{WDI} = constant f_{WDC} = 5 kHz		$t_{WDIerror}$	49		51	ms	A
16	**Watchdog Timing Relative to f_{WDC}**								
16.1	Minimum pulse duration for a guaranteed WDI input-pulse detection					2		cycles	A
16.2	Frequency range for a correct WDI signal				80		170	cycles	D
16.3	Hysteresis range at the WDI ok margins					1		cycle	A
16.4	Detection time for a stucked WDI signal (WDI dropout)	V_{WDI} = constant			250		251	cycles	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If V_S > 26 V the current has to be limited at 5 mA by an external resistor.

8. Protection Versus Transient Voltages According to ISO TR 7637-1 Level 4 (Except Pulse 5)

Pulse	Voltage	Source Resistance[1]	Rise Time	Duration	Amount
1	–110V	10Ω	100V/s	2 ms	15.000
2	+110V	10Ω	100V/s	0.05 ms	15.000
3a	–160V	50Ω	30V/ns	0.1 µs	1h
3b	+150V	50Ω	20V/ns	0.1 µs	1h
5	55V	2Ω	10V/ms	250 ms	20

Note: 1. In the case of the relay driver, the coil resistance of R_{min} = 150Ω has to be added to the source resistance.

9. Timing Diagrams

Figure 9-1. Watchdog in Too-fast Condition

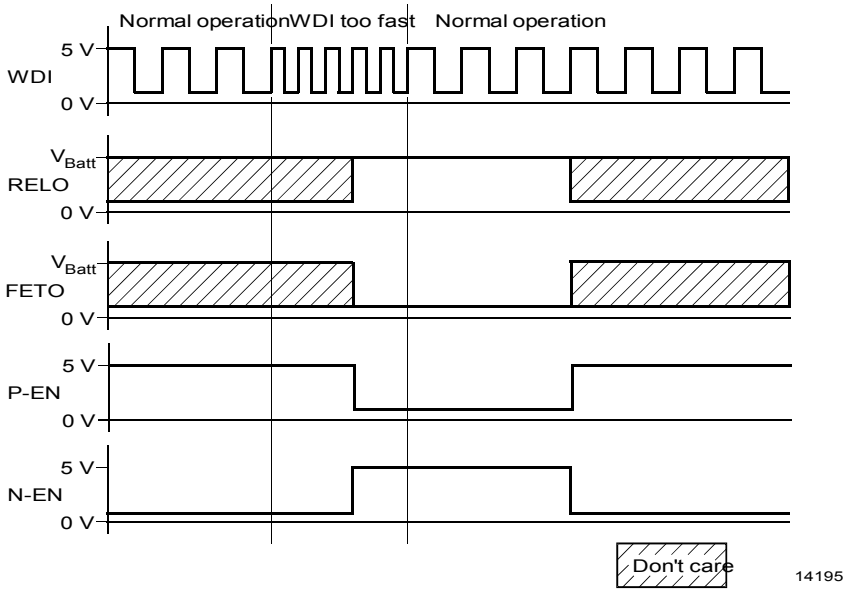


Figure 9-2. Watchdog in Too-slow Condition

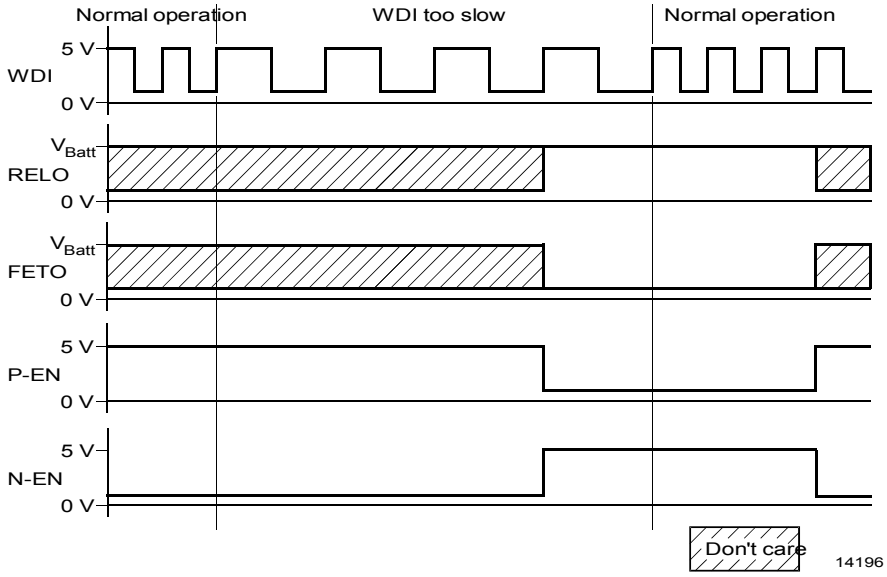


Figure 9-3. Overvoltage Condition

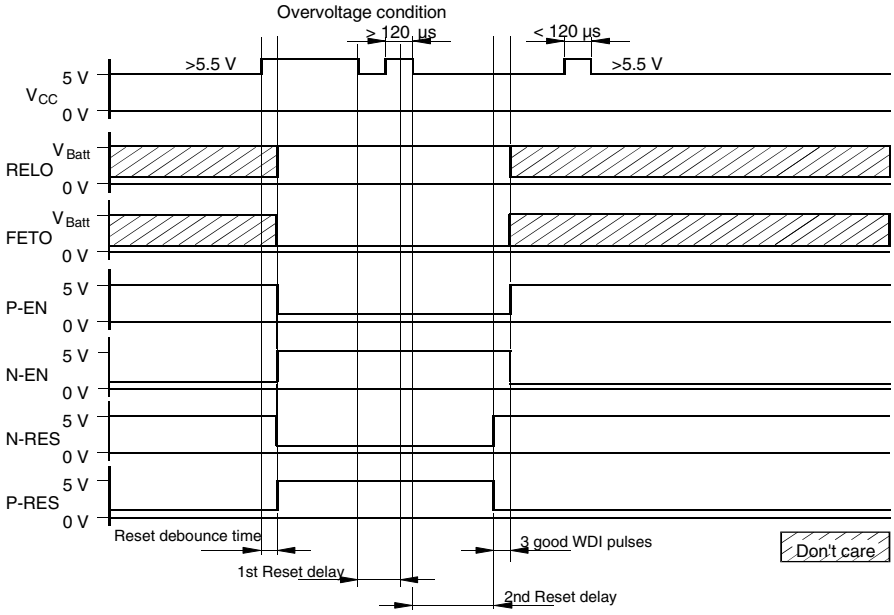


Figure 9-4. Undervoltage Condition

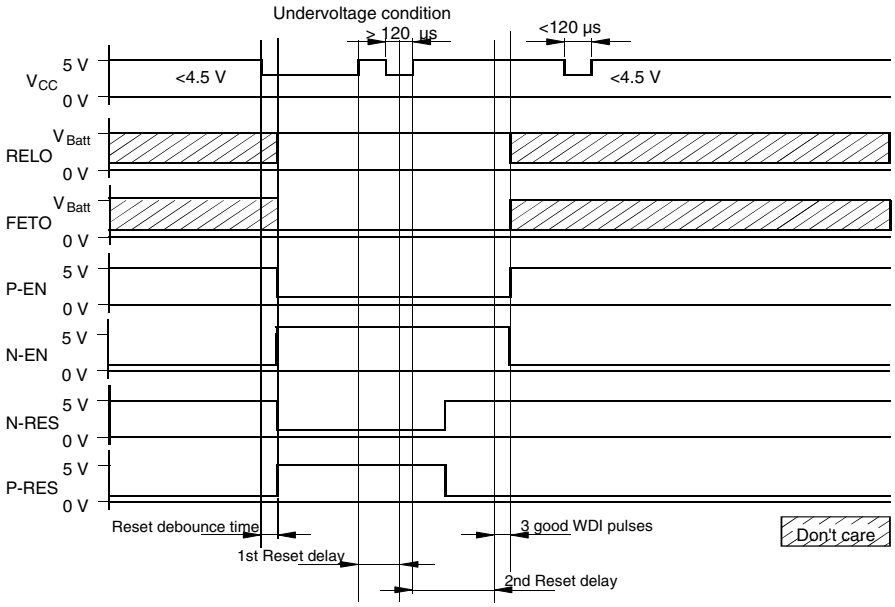
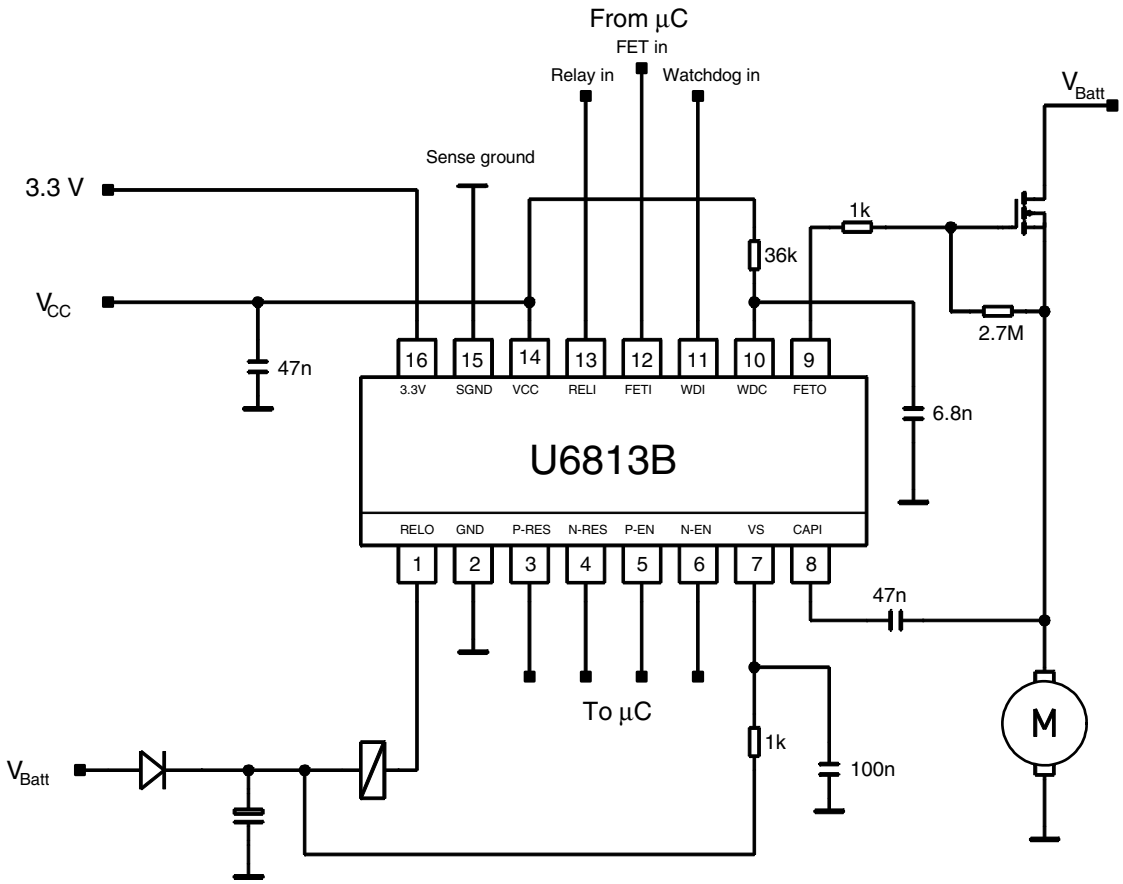


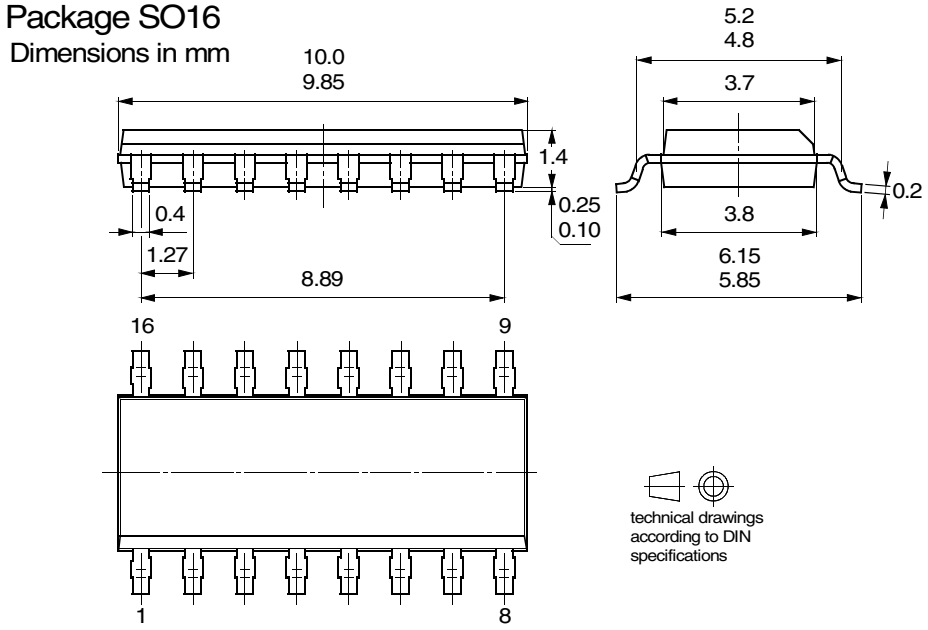
Figure 9-5. Application Circuit



10. Ordering Information

Extended Type Number	Package	Remarks
U6813B-MFPG3Y	SO16	Taped and reeled, Pb-free

11. Package Information



12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4543B-AUTO-10/05	• Put datasheet in a new template • Pb-free logo on page 1 added • New heading rows on Table “Absolute Maximum Ratings” on page 7 added • Table “Ordering Information” on page 15 changed

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